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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/580,625	05/24/2006	Raymond J. E. Hueting	GB03 0212 US	4378

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NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
HSIEH, HSIN YI	

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/580,625	HUETING ET AL.	
	Examiner	Art Unit	
	Hsin-Yi (Steven) Hsieh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 May 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE GURLEY
SUPERVISORY PATENT EXAMINER
AU 2811, TC 2800

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20060524*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The listing of references in the Search Report is not considered to be an information disclosure statement (IDS) complying with 37 CFR 1.98. 37 CFR 1.98(a)(2) requires a legible copy of: (1) each foreign patent; (2) each publication or that portion which caused it to be listed; (3) for each cited pending U.S. application, the application specification including claims, and any drawing of the application, or that portion of the application which caused it to be listed including any claims directed to that portion, unless the cited pending U.S. application is stored in the Image File Wrapper (IFW) system; and (4) all other information, or that portion which caused it to be listed. In addition, each IDS must include a list of all patents, publications, applications, or other information submitted for consideration by the Office (see 37 CFR 1.98(a)(1) and (b)), and MPEP § 609.04(a), subsection I. states, "the list ... must be submitted on a separate paper." Therefore, the references cited in the Search Report have not been considered. Applicant is advised that the date of submission of any item of information or any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the IDS, including all "statement" requirements of 37 CFR 1.97(e). See MPEP § 609.05(a).

3. The information disclosure statement filed 05/24/2006 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 42. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features of "the field plate electrode is connected to the source" of claim 13, and "a field plate terminal connected to the

field plate" of claim 14 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Trench insulated gate field effect transistor having a field plate electrode.

7. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: claim 9 recites "the thickness of the insulator thickness adjacent to the field plate electrode is greater than the thickness of the insulator adjacent to the gate electrode" and claim 12 recites "the field plate oxide thickness is in the range 0.6 to 1 micron and the gate oxide thickness is in the range 0.2 to 0.5 micron", while these limitations are not disclosed anywhere in the specification other than the claims. There is no proper support for these limitations.

Claim Objections

8. Claims 1-14 are objected to because of the following informalities:

a. Claim 1 recites "drain regions regions extend" in the 9th line. Changing to "drain regions extend" is suggested.

b. Claims 1 and 8 recite "first conductivity type" and "second conductivity type" without the proper articles: "a" should be used for the first referral and "the/said" for the latter referrals.

c. Claim 1 recites "each trench" in the 13th line, "the field plate" in the 19th line, "the gate" in the 19th line, and "trenches" in the 20th line. Changing these limitations to "each insulated trench", "the conductive field plate electrode", "the conductive gate electrode", and "the insulated trenches", respectively, is suggested.

d. Claim 2 recites "the gate electrode" in the second line. Changing this limitation to "the conductive gate electrode" is suggested.

e. Claim 3 recites "the gate electrode" in the second line and 'the trench" in the third line. Changing these limitations to "the conductive gate electrode" and "the insulated trench", respectively, is suggested.

f. Claim 4 recites "the break down voltage" in the second line. Changing this limitation to "a break down voltage" is suggested.

g. Claim 5 recites "trenches" in the third line. Changing this limitation to "the insulated trenches" is suggested.

h. Claim 7 recites "the source contact" in the 4th line. Changing this limitation to "a source contact" is suggested.

i. Claim 9 recites "the thickness of the insulator thickness adjacent". Changing this limitation to "the thickness of the insulator adjacent" is suggested.

j. Claim 9 recites "the field plate electrode" in the third line and 'the gate electrode" in the third line. Changing these limitations to "the conductive field plate electrode" and "the conductive gate electrode", respectively, is suggested.

k. Claim 11 recites 'the gate" in the last line. Changing this limitation to "the conductive gate electrode" is suggested.

l. Claim 12 recites "the field plate oxide" in the second line and 'the gate oxide" in the third line. Changing these limitations to "the field plate insulator" and "the gate insulator", respectively, is suggested.

m. Claim 13 recites "the field plate electrode" in the second line and 'the source" in the third line. Changing these limitations to "the conductive field plate electrode" and "the source region", respectively, is suggested.

n. Claim 14 recites "the field plate" in the third line and "the field plate voltage" in the fourth line. Changing these limitations to "the conductive field plate electrode" and "a field plate voltage", respectively, is suggested.

o. Claim 8 has a black line at the beginning of the third line of the claim. Removing the black line is suggested.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. Claims 9 and 12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 9 recites "the thickness of the insulator thickness adjacent to the field plate electrode is greater than the thickness of the insulator adjacent to the gate electrode" and claim 12 recites "the field plate oxide thickness is in the range 0.6 to 1 micron and the gate oxide thickness is in the range 0.2 to 0.5 micron", while these limitations are not disclosed anywhere in the specification other than the claims.

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 7-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

13. Claim 7 recites "a trench" in the second line of claim 7 and claim 8 recites "the trench" in the 4th line of claim 8, and both claims depend on claim 1. The trench recited in claims 7 and 8 is different from the trench recited in claim1 in light of the specification, which render claims 7 and 8 indefinite. It is recommended to use different terms for these different trenches to avoid the confusion.

14. Claim 8 is rejected because it depends on the rejected claim 7.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

17. **Claims 1, 4-7, 9-10, and 12-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. (EP 1168455 A2) as can be understood since claims 1-14 have been rejected under 35 U.S.C. 112.

18. Regarding **claim 1**, Omura et al. teach an insulated gate field effect transistor (power semiconductor switching element; [0001]), comprising: a semiconductor body (11, 12, 13 and 14; Fig. 2, paragraph [0023]) having opposed first and second major surfaces (the top surface of 13 and the bottom surface of 11; Fig. 2); a source region (source layer 14; Fig. 2, paragraph [0023]) of first conductivity type (n-type; paragraph [0023]) at the first major surface (the top surface of 13); a body region (well layer 13; Fig. 2, paragraph [0023]) of second conductivity type (p-type) opposite to the first conductivity type (n-type) under the source region (14; see Fig. 2); a drift region (drift layer 12; Fig. 2, paragraph [0023]) of first conductivity type (n-type; paragraph [0023]) under the body region (13; see Fig. 2); a drain region (semiconductor substrate 11; Fig. 2, paragraph [0023]) of first conductivity type (n-type) under the drift region (12; see Fig. 2), so that the source (14), body (13), drift (12) and drain regions (11) regions extend in that order from the first major surface (the top surface of 13) towards the second major surface (the bottom surface of 11); and insulated trenches (trench 15; Fig. 2, paragraph [0024]) extending from the first major surface (the top surface of 13) towards the second major surface (the bottom surface of 11) past the source region (14) and the body region (13) into the drift region (12), each trench (15) having sidewalls (see Fig. 2), and including insulator (first insulating film 16 and second insulating film 18; Fig. 2, paragraph [0024]) on the sidewalls (see Fig. 2), at least one conductive gate electrode (gate electrode 19; Fig. 2, paragraph [0024]) adjacent to the body region (13) separated from the body region (13) by a gate insulator (second insulating film 18;

Fig. 2, paragraph [0024]), and at least one conductive field plate electrode (buried electrode 17; Fig. 2, paragraph [0024]) adjacent to the drift region (12) separated from the drift region (12) by a field plate insulator (first insulating film 16; Fig. 2, paragraph [0024]), and a gate-field plate insulator (18) separating the field plate (17) from the gate (19), wherein the source regions (14) and trenches (15) define a pattern of cells across the first major surface (stripped pattern; Fig. 1, paragraph [0022]); and the doping concentration in the drift region (12) increases from the part of the drift region (12) adjacent to the body region (13) to the part of the drift region (12) adjacent to the drain region (11; see Fig. 15B, paragraph [0053]),

Omura et al. do not teach the doping concentration in the drift region (12) being at least 50 times greater adjacent to the drain region (11) than adjacent to the body region (13).

Parameters such as the doping concentration in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device performance, e.g. ON resistance and switching speed as disclosed by Omura et al. in paragraph [0003]. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to incorporate the doping concentration within the range as claimed in order to achieve desired device performance.

19. Regarding **claim 4**, Omura et al. do not teach an insulated gate field effect transistor according to claim 1 wherein the breakdown voltage is less than or equal to 30V.

Omura et al. teach a device with a breakdown voltage of 50V (paragraph [0045]). Omura et al. also teach that the breakdown voltage and the ON resistance satisfy the inequality: $Ron < 2.2 \times 10^{-5} Vb^{2.25}$.

Parameters such as the breakdown voltage and the ON resistance in the art of semiconductor manufacturing process are the tradeoff between the device's performance and reliability and are subject to changes due to the requirement of the application, e.g. whether the performance (lower ON resistance) is more important than the reliability (higher break down voltage). Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to lower the breakdown voltage to less than or equal to 30V as claimed in order to achieve a lower ON resistance to improve device performance.

20. Regarding **claim 5**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 wherein the pattern of cells defined by the source regions (14) and trenches (15) arranged across the first major surface (the top surface of 13) is a pattern in which cells repeat in more than one direction across the surface to form a three-dimensional cell structure (see Fig. 25).

21. Regarding **claim 6**, Omura et al. also teach an insulated gate field effect transistor according to claim 5 wherein the cells are arranged in a hexagonal pattern (see Fig. 25)

22. Regarding **claim 7**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 further comprising a trench (the trench formed between the interlevel dielectric films 22; Fig. 4; paragraph [0026]) filled with conductive material (the conductive material of the source electrode 21; Fig. 4, paragraph [0026]) extending through the source region (14) to the body region (13) to connect the source contact (source electrode 21) to the source region (14) and the body region (13; see Fig. 4).

23. Regarding **claim 9**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 wherein the thickness of the insulator (16; Fig. 2) thickness adjacent to the

field plate electrode (17) is greater than the thickness of the insulator (18) adjacent to the gate electrode (19; see Fig. 2, paragraph [0031]).

24. Regarding **claim 10**, Omura et al. do not teach an insulated gate field effect transistor according to claim 1 wherein the cell pitch is not greater than 1 micron.

Parameters such as the cell pitch in the art of semiconductor manufacturing process are subject to change due to the requirement of the device performance. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to use a cell pitch not greater than 1 micron as claimed to achieve the required performance.

25. Regarding **claim 12**, Omura et al. do not teach an insulated gate field effect transistor according to claim 1 wherein the field plate oxide (16) thickness is in the range 0.6 to 1 micron and the gate oxide thickness (18) is in the range 0.2 to 0.5 micron.

Omura et al. teach that the thickness of the field plate oxide (16) is determined by the breakdown voltage and the thickness of the gate oxide (18) is determined by the threshold voltage (paragraph [0031]) Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to have the thickness of the field plate oxide and the thickness of the gate oxide as claimed as a result of achieving a desired or required breakdown voltage and threshold voltage.

26. Regarding **claim 13**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 wherein the field plate electrode (17) is connected to the source (21; Fig. 3, paragraph [0026])

27. Regarding **claim 14**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 further comprising a field plate terminal connected to the field plate for

controlling the field plate voltage independently (this is implied in the paragraph [0027], where Omura et al. disclose a voltage applied to each buried electrode 17, which obviously need a terminal connected to the buried electrode 17 to control the voltage).

28. **Claims 2 and 11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. as applied to claim 1 above, and further in view of Onda et al. ("SIC Integrated MOSFETs" Physica Status Solidi (A), Applied Research, Berlin, DE, vol. 162, no. 1, 16 July 1997, pages 369-388) as can be understood since claims 1-14 have been rejected under 35 U.S.C. 112.

Omura et al. teach, regarding to **claim 11**, the first conductivity type is n-type (the conductivity type of the source region; paragraph [0023]), the second conductivity type is p-type (the conductivity type of the body region; paragraph [0023]).

Omura et al. do not teach, regarding to **claim 2**, the gate electrode is of conductive semiconductor doped to be the second conductivity type (i.e. p-type), and regarding to **claim 11**, the gate is of p-type doped polysilicon.

In the same field of endeavor of semiconductor device, Onda et al. teach the gate electrode is a p-type doped polysilicon (Fig. 1, page 371 line 27). Onda et al. also teach that p-type polysilicon is used to form an accumulation mode SiC trench MOSFET (page 371, lines 23-43).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Omura et al. and Onda et al. and use the gate taught by Onda et al., because an accumulation mode SiC trench MOSFET can be formed as taught by Onda et al.

29. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. as applied to claim 1 above, and further in view of Miyano et al. (JP 403211885A) as can be understood since claims 1-14 have been rejected under 35 U.S.C. 112.

Regarding **claim 3**, Omura et al. do not teach the gate electrode has side pieces spaced apart adjacent to the sidewalls on either side of the trench and a top piece spanning the gap between the side pieces.

In the same field of endeavor of semiconductor device, Miyano et al. teach the gate electrode (3; Fig. 1, Abstract) has side pieces spaced apart adjacent to the sidewalls on either side of the trench (a grove; Fig. 1, Abstract) and a top piece spanning the gap between the side pieces (see Fig. 1 of the shape of the gate electrode). Miyano et al. also teach the shape of the gate reduces the capacitance between the gate and the drain, and a high speed operation can be performed (Abstract).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Omura et al. and Miyano et al. and use the gate taught by Miyano et al., because the speed of the device can be improved as taught by Miyano et al.

30. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. as applied to claim 7 above, and further in view of Hshieh et al. (US 2001/0003367 A1).

Regarding **claim 8**, Omura et al. do not teach a doped contact region of second conductivity type in the body region in contact with the conductive material in the trench, the doping concentration in the doped contact region being higher than the doping in the rest of the body region.

In the same field of endeavor of vertical transistors, Hshieh et al. teach a doped contact region (P+ region 138; Fig. 2, paragraph [0025]) of second conductivity type (p type) in the body region (in the P-body region; Fig. 2, paragraph [0025]) in contact with the conductive material (source metal layer 160; Fig. 2, paragraph [0025]) in the trench (source contact openings 150; Fig. 2, paragraph [0025]), the doping concentration in the doped contact region being higher than the doping in the rest of the body region (the doping concentration of P+ region is higher than P region). Hshieh et al. also teach the doped contact region 138 is used to reduce the parasitic resistance (paragraph [0025]).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Omura et al. and Hshieh et al. and use the doped contact region taught by Hshieh et al., because the parasitic resistance can be reduced as taught by Hshieh et al.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsin-Yi (Steven) Hsieh whose telephone number is 571-270-3043. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HH
10/24/2007

LYNNE GURLEY
SUPERVISORY PATENT EXAMINER
AU 2811, TC 2800